

RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, MARCH 2022

FIRST YEAR [BATCH 2021-24]

COMPUTER SCIENCE (HONOURS)

Date : 10/03/2022

Time : 11 am – 1 pm

Paper : II [CC 2]

Full Marks : 50

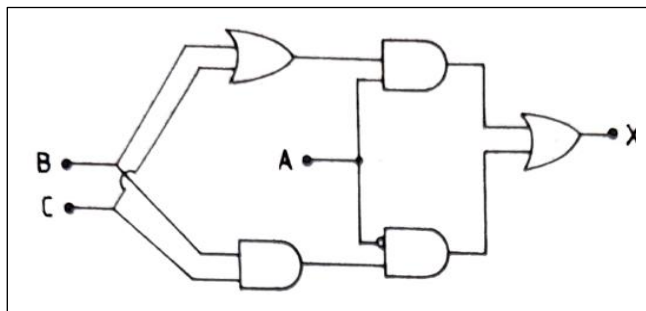
Group : A

Answer **any two** questions from question no. 1 to 3: [2×2.5]

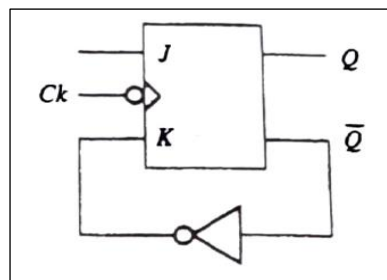
1. Design an S-R latch using only two NAND gates. Compare its forbidden state with that of S-R latch designed with only two NOR gates. [1+1.5]
2. What do you mean by Don't Care states? Compare them with permitted states and also discuss why sometimes it is necessary for getting most simplified logic functions. [1+1.5]
3. What is race-around and for which type of latches it is unavoidable? What method can be used to encounter race-around? [1.5+1]

Answer **any two** questions from question no. 4 to 6: [2×5]

4. Using a single OR gate and few NOT gates to implement the AND function for two input Boolean variables. For the following logic circuit obtain the relation between input and output: [2+3]



5. Using T-type flip-flops and few logic gates design a circuit which is capable of dividing the clock frequency by 5. The following logic circuit uses a J-K flip-flop. There is one input J, and the output is Q. Find the output Q_{n+1} , after the clock pulse in terms of the input J and the output before the clock pulse Q_n . [3+2]



6. What is MUX? Cascade two 4 X 1 MUXs (preferably IC 74153) to have one 8 X 1 MUX functionality. Use a 16 X 1 MUX for implementing the following logic function: [1+1+3]

$$F(A_3, A_2, A_1, A_0) = A_2 \cdot \overline{A_1} \cdot A_0 + A_3 \cdot \overline{A_2} \cdot \overline{A_0} + \overline{A_3} \cdot A_0$$

Answer **any one** question from question no. 7 and 8: [1×10]

7. a) Compare Ring Counter and Johnson Counter. Why these types of counters are designed with D flip-flops instead of using T flip-flops? [2+2]

- b) “Synchronous counters are working in synchronisation with external clock pulses, but asynchronous counters are not. That means asynchronous counters do not need any external clock pulses.” – is this true? Explain your answer in brief. [2]
- c) Design a Mod-6 asynchronous counter which have both of UP and DOWN count facility. [4]
8. a) Use Adder Chip (IC 7483 or 74283) for converting any single digit BCD number to corresponding 10's complement. [2]
- b) Use Adder Chips (IC 7483 or 74283) for designing a circuit which is capable of performing 2's complement addition and subtraction of two four bit numbers. Discuss the working of the circuit in details. [2+4]
- c) Design a comparator circuit using IC 7485 which can check a given four bit number is valid BCD or not. [2]

Group :B

Answer **any two** questions from question no. 9 to 11: [2×2.5]

9. What is tri-state device? Explain the working principle with a suitable block diagram. [1+1.5]
10. What do you mean by flag registers? Write down functions of flag registers. [1+1.5]
11. Write down the differences between SRAM and DRAM.

Answer **any two** questions from question no. 12 to 14: [2×5]

12. Discuss Von-Neumann architecture with a suitable diagram. [5]
13. a) Explain I/O operation of DMA with a suitable block diagram.
- b) What do you mean by cache-hit and cache-miss. [3+2]
14. Why do we need ADC and DAC? Draw a Weighted-Resistor type DAC which can convert a 6-bit digital data to equivalent analog signal. If the resistance connected at the LSB terminal is $100\text{ K}\Omega$, then find the resistance to be connected at the MSB terminal of that 6-bit DAC. [2+2+1]

Answer **any one** question from question no. 15 and 16: [1×10]

15. a) Write down the differences between the followings:
- Hardwired and microprogrammed control unit
 - Horizontal and vertical microinstruction
 - RISC and CISC
- b) Explain displacement addressing mode. [(2+2+3)+3]
16. a) Define the followings:
- Direct access
 - Access time
 - Transfer rate
- b) Explain direct mapping technique with a suitable block diagram.
- c) How would you justify the importance of pipelining?
- d) Write down different bus arbitration mechanisms. [(1+1+1)+3+2+2]

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